THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KATSUHIRO TSUKAMOTO

Appeal No. 96-1549
Application 08/296,988[1]

ON BRIEF

Before THOMAS, MARTIN, and BARRETT, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claim 10, Appellant's sole pending claim,

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[1] Application for patent filed August 26, 1994. According to Appellant, the application is a continuation of Application 07/738,648, filed July 31, 1991 (now abandoned), which is a continuation of Application 07/662,989, filed February 28, 1991 (now Patent No. 5,047,818), which is a continuation of Application 07/146,686, filed January 20, 1988 (now abandoned).

under 35 U.S.C. § 103 for obviousness over the prior art.[2] We reverse.

The invention is a semiconductor memory device which includes a continuous buried layer which serves as a barrier against "-ray induced carriers.

Claim 10, the sole appealed claim, reads as follows:

10. A semiconductor memory device including a memory sell having a write/read transistor and a charge storage capacitor comprising:

a semiconductor substrate formed of a material having a first conductivity type and first impurity concentration, said substrate having a main surface;

a field oxide isolation film formed on said main surface for isolating semiconductor elements from each other;

a pair of regions of a second conductivity type of said write/read transistor formed on said main surface, a first region of said pair of regions being connected with a bit line and the second region of said pair of regions being connected with one electrode of said charge storage capacitor;

a gate formed on said main surface between said pair of regions of said write/read transistor; and

a continuous buried layer of the first conductivity type formed to stop " particles having a second impurity concentration higher than said first impurity concentration of said substrate and being continuously formed in said substrate beneath said gate and said pair of regions of said write/read transistor as well as beneath said field oxide isolation film,

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[2] This is the second § 134 appeal in this application. In the first appeal (Appeal No. 93-3432), the Board affirmed the § 103 rejection of a different claim, i.e., claim 9.

wherein said continuous buried layer has a first peak position of impurity concentration beneath said field oxide isolation film and a second peak position of impurity concentration beneath said gate and said first region of said pair of regions, a first depth from said main surface to said first peak position being less than a second depth from said main surface to said second peak position, and

said continuous buried layer has a lower surface arranged so that the entire lower surface is in contact with said substrate material.

The only reference relied on by the examiner in the Answer is:

Wordeman et al. (Wordeman), A Buried N-Grid for Protection Against Radiation Induced Charge Collection in Electronic Circuits, IEDM Tech. Dig., pp. 40-43, 1981.

Although the final Office action (at 3) additionally mentions Bakeman, Jr., et al. U.S. Patent 4,506,436 (Bakeman) in response to Appellant's arguments, the Answer specifically states (at 5) that Bakeman is not used in the rejection.[3] Accordingly, Bakeman has not been considered.

Claim 10 stands rejected for obviousness over the DRAM cell structure shown in Figure 6 of Wordeman, which includes, inter alia, a buried grid of n-type material (labeled "BURIED n-LAYER") and a buried continuous layer of p-type material (labeled "BURIED

[3] Bakeman was relied on in the previous appeal, in which the Board affirmed a rejection of claim 9 for obviousness over Wordeman in view of Bakeman.

p-LAYER)." As best shown in Figure 3b, the buried p-type layer has deeper portions or dimples which fill in the holes in the n-type grid and has shallower portions which overlie the n-type material of the grid. Figure 6 shows that when this arrangement is used in a DRAM cell, the n-type grid and p-type layer are positioned such that the deeper portions or dimples of the p-type layer lie under the n-type bit lines and FET channels, where capacitance is to be minimized, and the shallower portions of the p-type layer lie under the storage nodes, where an increase in capacitance is desirable (Wordeman at 42-43).

Appellant argues that Wordeman's buried p-type layer fails to satisfy the claim in two respects, the first being that Wordeman does not teach that the buried p-layer by itself "would be adequate to substantially reduce the soft-error rate, as taught by the present invention" (Br. at 7). This argument fails because the claim language "formed to stop " particles" does not require that substantially all " particles be stopped and because Wordeman discloses (at 41, 2d col., item 3) that the p-type layer

> . . . blocks the radiation-generated minority carriers from diffusing up through the [grid] holes (due to the field in the high-low junction formed between the low doped substrate and the high p-doping in the hole). These carriers diffuse sideways to be collected in the n-grid.

Appellant's second argument is that the buried p-type layer does not "ha[ve] a lower surface arranged so that the entire lower surface is in contact with said substrate material," as required by the claim. The examiner argues that this limitation is satisfied because the n-type grid material that underlies the p-type layer is part of the substrate material (Answer at 3). We agree with Appellant that after the substrate material is converted to n-type grid material, it is no longer part of the substrate in the sense of the claim (Reply Br. at 1-2), which recites a "substrate formed of a material having a first conductivity type and first impurity concentration." We therefore agree with Appellant that the entire lower surface of Wordeman's buried p-type layer is not in contact with the substrate material, as required by the claim.

The examiner alternatively notes (Answer at 4-5) that the Board in the previous appeal determined that it would have been obvious to omit Wordeman's n-type grid altogether, in which case the p-type layer would have its entire lower surface in contact with the substrate. Claim 9 in that appeal included a limitation ("wherein the entire buried layer has a lower surface in contact with said substrate") which is similar to the limitation of

claim 10 at issue in this appeal. In affirming a rejection of claim 9 for obviousness over Wordeman in view of Bakeman, the Board stated:

> . . . [W]e note that it is the upper surface of the buried P layer that provides all of the advantages described by appellant in the specification. As indicated supra, the upper surface of the buried P layer is located at one distance from the capacitor region, and is located at another distance from the transistor region. The specification is completely silent concerning any advantage that is gained by having the entire lower surface of the buried P layer in contact with the substrate. For this reason, we find that it would have been manifestly obvious to one of ordinary skill in the art to eliminate the N layer that lies buried under a portion of the buried P layer in Figure 6 of Wordeman. [Paper No. 24, at 5.]

Appellant argues that when considered without reference to Appellant's specification, Wordeman fails to suggest that the n-type grid can be omitted and the p-type layer used alone to collect radiation-generated minority carriers. We agree. In Wordeman, the function of collecting the radiation-generated minority carriers is performed primarily by the n-type buried grid (Wordeman at 40, 2d col.); the primary function of Wordeman's p-type layer is to prevent "punch through" to the n-type grid from reverse-biased surface elements (Wordeman at 41, 1st col.). Although, as noted above, Wordeman discloses that the p-type layer additionally prevents minority carriers from passing through the grid openings and diffuses them sideways to be

collected by the grid, Wordeman does not suggest that the p-type layer would be capable, in the absence of the n-type grid, of blocking enough minority carriers to make it feasible to omit the n-type grid.

For the foregoing reasons, the rejection of claim 10 under 35 U.S.C. § 103 as unpatentable over Wordeman is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
JOHN C. MARTIN Administrative Patent Judge	) BOARD OF PATENT)) APPEALS AND)) INTERFERENCES
LEE E. BARRETT Administrative Patent Judge	)

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